REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-69 are pending. Claims 1-69 have been rejected.

Claims 1, 3, 5, 34, 36, and 38 have been amended. Claims 2 and 35 have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Applicants reserve all rights with respect to the applicability of the Doctrine of Equivalents.

The Examiner objected to the specification. The Examiner stated that "Applicant should amend claim 34 to claim computer readable media (as opposed to machine readable media) to match the specification." (Office Action 4/14/08, p. 2).

Without necessarily agreeing with the Examiner's objection to the specification, applicants have amended claim 34 to replace "machine" to "computer", as the Examiner requested.

The Examiner objected to claims 1 and 34 because of informalities.

Applicants have amended claims 1 and 34 in light of the Examiner's objection.

Therefore, applicants submit that the Examiner's objections with respect to claims 1 and 34 have been overcome.

Claims 1-2, 5-7, 11-14, 17-20, 23-30, 32-35, 38-40, 44-47, 50-53, 56-63, 65-66, and 68 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,446,198 to Sazegari (hereinafter "Sazegari").

Amended claim 1 reads as follows:

A method for execution by a microprocessor in response to receiving a single instruction, the method comprising:

receiving a string of bits having a plurality of segments;

receiving a plurality of data elements specifying the plurality of segments in the string of bits;

generating a plurality of indices based on the plurality of data elements, wherein a first one of the plurality of indices is generated from retrieving a first bit segment from the string of bits according to a first one of the plurality of data elements;

receiving a configuration indicator, wherein the configuration indicator indicates how to configure a plurality of look-up units into one or more look-up tables for execution of the single instruction;

configuring the plurality of look-up units into one or more look-up tables according to the configuration indicator;

looking up simultaneously a plurality of entries from the one or more look-up tables using the plurality of indices, the one or more look-up tables [[is]] configured from the plurality of look-up units, wherein each of said plurality of look-up units is a memory unit that is separate and distinct from others of said plurality of look-up units and is individually accessible independent of operations of the other look-up units; and

combining the plurality of entries into a first result;

wherein the above operations are performed in response to the microprocessor receiving the single instruction.

(emphasis added)

Sazegari describes logically dividing a large table into a number of smaller tables that can be indexed with a permute instruction (col. 2, lines 17-43). Sazegari discloses that the permute instruction uses the mask values from the register 26 to assign corresponding values of the operands stored in registers 28 and 30 to a result register 32. (Figure 3, col. 4, lines 5-24). More specifically, Sazegari discloses the following:

> For table lookup operations, the permute instruction can be used to perform 16 simultaneous lookup operations on a 32-byte entry table. FIG. 4 illustrates such a table 34, which consists of two 16-byte vectors, data1 and data2. Each vector can be stored in one register of the CPU. The permute instruction can be used to simultaneously read 16 values from these two vectors, in accordance with index values in a register 36, and store the 16 output results in sequential order in another register 38.

(Sazegari, col. 4, lines 24-32) (emphasis added)

In particular, Sazegari discloses the following:

> Since the permute instruction selects bytes from two registers which each have a maximum length of 128 bits, or 16 bytes, it is capable of selecting from among 32 different bytes, or entries in the table. Each of these 32 different entries can be uniquely identified with five bits of each byte in the index register 36. Consequently, the three most significant bits of each byte in this register are unused when the permute instruction is employed for table lookups, as described above. In accordance with the present invention, these three unused bits are employed to expand the size of a table which can be indexed by means of the permute instruction. This result is accomplished through the use of a "select" instruction in combination with multiple permute operations.

(Sazegari, col. 4, lines 33-46) (emphasis added)

Thus, Sazegari merely discloses identifying each of the entries in the look-up table with five bits of each byte in the index register. In contrast, amended claim 1 refers to receiving a plurality of data elements specifying the plurality of segments in the string of bits; and generating a plurality of indices based on the plurality of data elements, wherein a first one of the plurality of indices is generated from retrieving a first bit segment from the string of bits according to a first one of the plurality of data elements.

Because Sazegari fails to disclose all limitations of amended claim 1, applicants respectfully submit that claim 1, as amended, is not anticipated by Sazegari under 35 U.S.C. § 102(e).

For at least the same reasons, as discussed above with respect to amended claim 1, applicants respectfully submit that claims 5-7, 11-14, 17-20, 23-30, 32-35, 38-40, 44-47, 50-53, 56-63, 65-66, and 68 are not anticipated by Sazegari under 35 U.S.C. § 102(e).

The Examiner rejected claims 3-4, 8-10, 15-16, 21-22, 31, 36-37, 41-43, 48-49, 54-55, 64 and 69 under 35 U.S.C. § 103(a) as being obvious over Sazegari.

As set forth above, Sazegari discloses identifying each of the entries in the look-up table with the bits in the index register. Sazegari fails to disclose, teach, or suggest receiving a plurality of data elements specifying the plurality of segments in the string of bits; and generating a plurality of indices based on the plurality of data elements, wherein a first one of the plurality of indices is generated from retrieving a first bit segment from the string of bits according to a first one of the plurality of data elements, as recited in amended claim 1.

Given that claims 3-4, 8-10, 15-16, 21-22, 31, 36-37, 41-43, 48-49, 54-55, 64 and 69 contain the limitations that are similar to those limitations discussed with respect to amended claim 1, applicants respectfully submit that claims 3-4, 8-10, 15-16, 21-22, 31, 36-37, 41-43, 48-49, 54-55, 64 and 69 are not obvious under 35 U.S.C. § 103(a) over Sazegari.

The Examiner rejected claim 67 under 35 U.S.C. § 103(a) as being unpatentable over Sazegari in view of U.S. Patent No. 5,526,501 to Shams ("Shams").

It is respectfully submitted that Shams also fails to disclose, teach, or suggest receiving a plurality of data elements specifying the plurality of segments in the string of bits; and generating a plurality of indices based on the plurality of data elements, wherein a first one of the plurality of indices is generated from retrieving a first bit segment from the string of bits according to a first one of the plurality of data elements, as recited in amended claim 1.

Furthermore, even if the addressing scheme of Shams were incorporated into a vectorized table lookup of Sazegari, such a combination would still lack receiving a plurality of data elements specifying the plurality of segments in the string of bits; and

generating a plurality of indices based on the plurality of data elements, wherein a first one of the plurality of indices is generated from retrieving a first bit segment from the string of bits according to a first one of the plurality of data elements, as recited in amended claim 1.

Given that claim 67 depends from amended claim 1, and adds additional limitations, applicants respectfully submit that claim 67 is not obvious under 35 U.S.C. § 103(a) over Sazegari in view of Shams.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 022666.

Respectfully submitted,

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